Serial No.: 09/644,464

## REMARKS

Claims 1, 3-14 and 16-22 are pending in the application upon entry of this amendment. Claims 1, 7, 11, 14 and 20 have been amended herein. Claims 23 has been canceled. Favorable reconsideration of the application, as amended, is respectfully requested.

### *I. REJECTION OF CLAIMS 1-23 UNDER 35 USC §112, 2nd ¶*

Claims 1-23 remain rejected under 35 USC §112, second paragraph, as being indefinite. Specifically, the Examiner notes that the claims are still indefinite with respect to points a (i thru iii) as set forth on pages 2-3 of the Office Action.

Regarding points a (i and iii), the claims have been amended as noted above in order to address the Examiner's concerns.

As for point a (ii), applicants respectfully request clarification. Claim 14, line 3 does not appear to include the phrase "an address". Applicants are uncertain exactly what changes the Examiner feels are appropriate.

For at least the above reasons, applicants respectfully request that the rejection of claims 1-23 be withdrawn.

### *II. REJECTION OF CLAIMS 1, 3-14 AND 16-23 UNDER 35 USC §102(b)*

Claims 1, 3-14 and 16-23 remain rejected under 35 USC §102(b) based on *Firoozmand et al.* This rejection is respectfully traversed for at least the following reasons.

As noted in applicants' previous response, claims 1 and 14 recite the feature of the invention whereby the priority resolution circuit continually retrieves data from the register to determine a highest priority data frame in the buffer memory and *replaces the address previously provided to the frame transmission circuit if a higher priority frame becomes available*. Similarly, claim 10 recites a method which includes

*overwriting the address of the highest priority data frame with an address of a new highest priority data frame if a new higher yet priority data frame becomes available.*

The Examiner contends that *Firoozmand et al.* teaches such feature. The Examiner contends that *Firoozmand et al.* teaching a priority resolution circuit which continually retrieves data from the register to determine the highest priority data frame in the buffer memory. More specifically, the Examiner contends that *Firoozmand et al.* teaches that the priority resolution circuit continually retrieves the data *and replaces the address previously provided to the frame transmission circuit if a higher priority frame becomes available*. Applicants respectfully disagree, and will address each of the Examiner's points below.

*i.*

Regarding Column 13, lines 13-16; Fig. 16, the Examiner notes that synchronous data in *Firoozmand et al.* have higher priority over asynchronous data. The Examiner further notes that it is well known in the art that different data packets with varying priorities arrive at random times at the buffers. Applicants agree with the Examiner in this regard.

The Examiner goes on to state that ergo, continuous monitoring and retrieval of data packets based on priorities for transmission from the buffers is realized. To the extent that the Examiner is stating that it is well known in the art to continue to sense and provide higher priority data packets to the transmission circuit ahead of lower priority data packets, applicants again agree with the Examiner.

However, claims 1, 10 and 14 refer to continually retrieving data from the register to determine a highest priority data frame in the buffer memory and *replacing the address previously provided to the frame transmission circuit if a higher priority frame becomes available*. As applicants described in their previous response, the present invention is addressing the front of line blocking which occurs when the frame transmission circuit is provided with the address of the highest priority data frame and

then, *prior* to the frame transmission circuit actually transmitting the highest priority data frame, an even higher priority data frame is placed in the buffer memory.

According to the present invention, the address of the highest priority data frame provided to the frame transmission circuit is *replaced* with the address of the data frame now having an even higher priority. This way, when the frame transmission circuit is eventually granted access to the system bus, etc., the data frame having the even higher priority will be transmitted *before* the original highest priority data frame.

In *Firoozmand et al.* as well as the other conventional art referred to by the Examiner, the address of the highest priority data frame provided to the frame transmission circuit is not *replaced* with the address of the data frame now having an even higher priority. Rather, the frame transmission circuit retains the address of the highest priority data frame until the frame transmission circuit aquires access to the system bus, etc. and the highest priority data frame is transmitted. *Then*, the frame transmission circuit is subsequently provided with the address of the data frame having the even higher priority. The frame transmission circuit then transmits the data frame having the even higher priority.

Thus, in *Firoozmand et al.* the original highest priority data frame will still be transmitted prior to the data frame having the even higher priority. This front of line blocking situation is exactly opposite of the claimed invention. This is because the address provided to the frame transmission circuit in *Firoozmand et al.* is not being *replaced* in the event an even higher priority data frame is found in the buffer memory. Rather, the address of the even higher priority data frame is simply the next, or subsequent, address provided to the frame transmission circuit.

It will therefore be appreciated that Column 13, lines 13-17 of *Firoozmand et al.* simply relates to the priority at which packets are transmitted. Specifically, *Firoozmand et al.* describes how, when the transmitting device receives the token, the transmitting device transmits the synchronous data first. This is because the synchronous data has higher priority than non-synchronous data. Such transmission of the synchronous data

before non-synchronous data based on priority is very conventional and not the focus of the invention. There is no replacing of the address provided to the frame transmission circuit as discussed above.

*ii.*

Regarding Column 8, lines 10-40, the Examiner notes that "when a new data packet coming in from synchronous queue as is done in *Firoozmand* it gets a higher priority and 'jump' ahead of the remainder of the packets are currently present (if any), and gets processed.

Again, applicants agree with the Examiner that new data packets from the synchronous queue in *Firoozmand et al.* have higher priority and "jump" ahead of the remainder of the packets which are currently present. This is the same general priority scheme that is well known in the art as pointed out by the Examiner and discussed above.

Column 8, lines 10-40 of *Firoozmand et al.* discusses operation of the transmit section 152 in the DMA controller 124. The transmit section 152 transfers data stored therein to the output buffer memory 126 via an interface 150. (Col. 7, lns. 46-64; Fig. 8). A packet buffer management circuit 156 indicates to the medium access controller 120 what type of data is present in the transmit section, so as to load the buffer memory 126 in appropriate queues depending on the priority in accordance with the FIFO specifications.

The packet buffer management circuit 156 prioritizes command requests, transmit requests from the FIFO 152 and receive requests from the FIFO 154. The management circuit then issues commands to a system memory interface 160 to grant either transmits or receives or to process one of the commands. Transmit section FIFO 152 maintains all transmit queues and prioritizes operations in a predetermined priority. The transmit section FIFO 152 carries out byte ordering and data gathering, and

formats the data into FIFO oriented packets to be processed by the medium access controller 120.

With respect to packets transmitted from the transmit section FIFO 152 to the buffer memory 126, *Firoozmand et al.* teaches that the packet buffer management circuit 156 prioritizes the requests. The transmit section FIFO 152 maintains all transmit queues and prioritizes operations in a predetermined priority. (Column 8, lines 1-40).

The Examiner has not shown where in *Firoozmand et al.* it is taught or suggested that the transmit section FIFO 152 or the packet buffer management circuit 156 include any type of priority resolution circuit that continually retrieves data from the register to determine a highest priority data frame in the buffer memory and *replaces* the address previously provided to the frame transmission circuit *if a higher priority frame becomes available*.

Frankly, *Firoozmand et al.* has not been shown to even describe the priority resolution operation therein in sufficient detail that it could even be suggested that *Firoozmand et al.* teaches the claimed invention. Again, prioritization between data frames (e.g., synchronous vs. asynchronous) is not new and nor is it considered the invention. Rather, the invention relates the manner in which a data frame, previously slated for transmission by virtue of its address being provided to a priority resolution circuit so that the data frame is made available to the media access controller for transmitting, is not transmitted by virtue of its address being *replaced* by an address of a higher priority frame as discussed above. There simply is no such teaching or suggestion in *Firoozmand et al.*

*iii.*

Regarding "locking up" in *Firoozmand et al.*, the Examiner submits that the prevention of "locking up" in *Firoozmand et al.* is related to the front of line blocking

problem which the applicants are trying to solve. Applicants respectfully disagree in this regard.

*Firoozmand et al.* is concerned with "lock up" as pointed out by the Examiner. However, such "lock up" does not involve the front of line problem addressed by the present invention. More importantly, such "lock up" does not in any way involve continually retrieving data from a register to determine a highest priority data frame in the buffer memory and replacing the address previously provided to a frame transmission circuit if a higher priority frame becomes available, as recited in claims 1, 10 and 14.

Specifically, Firoozmand describes how the FIFO memory "locks up" when the amount of storage remaining available in the logical FIFO containing the queue, is less than the storage capacity of the physical FIFO. (Col. 2, lns. 17-23). *Firoozmand et al.* describes the network DMA controller 124 as designed to monitor the FIFO queue. If the queue becomes full, the packet buffer management circuit 156 locks the queue to finish emptying the current FIFO and to suspend the queue. If a transfer is incomplete, the circuit 156 continues with other pending transfers until receiving a signal that the queue becomes unlocked. Such "locking" and "flushing out" of the queue in no way relates to the presently claimed invention whereby an address provided by the priority resolution circuit is replaced with another address if a higher priority frame becomes available.

Again, the present invention is not concerned with basic prioritization as repeatedly referred to by the Examiner. Rather, the present invention addresses the front of line blocking problem associated with basic prioritization. The present invention avoids such problem by virtue of a unique configuration whereby the priority resolution circuit continually retrieves data from the register to determine a highest priority data frame in the buffer memory and *replaces* the address previously provided to the frame transmission circuit if a higher priority frame becomes available. Withdrawal of the

rejection of claims 1, 10, 14 and the claims dependent therefrom is respectfully requested.

## *III. CONCLUSION*

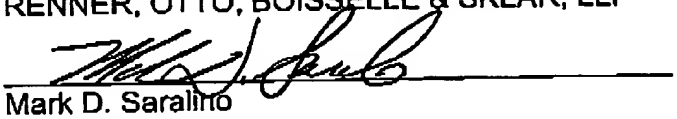
Accordingly, all claims are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP



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